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Applicant(s): KAMALESH K. SRIVASTAVA ET AL.

Docket No.
FIS920030359US1

Application No.	Filing Date	Examiner	Group Art Unit
10/708,649	05/17/2004	THERESA T. DOAN	2814

Invention: METHOD FOR FORMING ROBUST SOLDER INTERCONNECT STRUCTURES BY REDUCING EFFECTS OF SEED LAYER

I hereby certify that this Response to Restriction Requirement
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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

APPLICANT:	KAMALESH K. SRIVASTAVA ET AL.	) Group Art Unit: 2814
SERIAL NUMBER:	10/708,649	) Examiner: Theresa T. Doan
FILED:	May 17, 2004	) Confirmation No. 2648
FOR:	METHOD FOR FORMING ROBUST SOLDER INTERCONNECT STRUCTURES BY REDUCING EFFECTS OF SEED LAYER	)

Commissioner For Patents
P.O. Box 1450
Alexandria, VA. 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

In response to the restriction requirement mailed on May 2, 2005, and in accordance with the provisions under 37 CFR § 1.115 and 1.143, the Applicants submit the following election for further prosecution on the merits:

Election:

Applicants hereby elect, without traverse, Group II, claims 6-20, a method for forming an interconnect structure comprising annealing the semiconductor device as to cause atoms from the barrier layer to diffuse into the seed layer there underneath, wherein the annealing causes diffused regions of the seed layer to have an altered electrical resistivity and electrode potential with respect to undiffused regions of the seed layer.